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The signal flow graph based approach to the analysis and synthesis of complex combinational logic circuits

Contemporary MOS electronic technology enables to realize multi-input and multi-output combinational systems composed of logic gates as integrated discrete components. However, to realize complex logic functions more effective with respect to the number of switching elements can be a VLSI circuit of the architecture determined by an appropriate planar signal flow graph in which each branch X_1, X_2, \dots, X_n represents a single logic function dependent on some binary input signals A, B, C, \dots . This means that any branch of the circuit (graph) is (or is not) open, i.e. conducting electric current only for certain logical input states of A, B, C, \dots . In this work the signal flow graphs formalism is applied to the problem of analysis and synthesis of such VLSI systems [1,2,3].

It is relatively easy to determine logic functions realized by a given complex circuit. At the first step of the analysis the iterative reduction procedure of the graph structure can be done by replacing all pairs of branches X_i, X_j connected in parallel (or in series) by equivalent branches $X_i + X_j$ (or $X_i \wedge X_j$). In the result an irreducible signal flow graph is obtained. Then, to determine its logic functions all conducting branches of the graph should be taken into account. To do that it suffices to notice that each conducting path $X_{i1} \rightarrow X_{i2} \rightarrow \dots \rightarrow X_{ik}$ between a determined biased node and a given output node has an additive contribution to the output logic function in the disjunctive form. Finally, by the use of standard methods, the obtained logic function can be simplified and transformed to the form convenient for its practical realization.

The problem of synthesis of a VLSI circuit realizing given logic functions is more complex because both a suitable geometric structure of the graph and the logic functions of its branches are to be determined. In this work a simplified problem of synthesis is formulated for irreducible planar graphs with branches containing single switching elements (NO — normally open or NC — normally closed switch).

References

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The application of differential inclusions to the problem of stability of uncertain dynamical systems

Robust stability is a desired property of real dynamical and control systems. There are known several criteria for robustness of systems with interval, random or uncertain parameters based on the stability theory of differential equations and algebraic methods. In particular, the Kharitonov's algebraic criterion enables to verify stability of linear interval systems [1].

In this work the problem of stability of linear dynamical systems with uncertain parameters is formulated in terms of differential inclusions of the form

$$d\mathbf{x}/dt \in \{\mathbf{A}_0\mathbf{x} + z_1\mathbf{A}_1\mathbf{x} + z_2\mathbf{A}_2\mathbf{x} + \dots + z_k\mathbf{A}_k\mathbf{x} : |z_i(t)| < \alpha_i, i = 1, 2, \dots, k\}, \mathbf{x} \in \mathbb{R}^n,$$

where z_1, \dots, z_k are bounded time functions determining non-stationary system uncertainty. Fundamental difference between interval and uncertain parameters is pointed out.

Using the second method of Lyapunov and the conception of the stability index [2] it is proved that the limit values $\alpha_i, i = 1, 2, \dots, k$, of the uncertain parameters of a linear system determine its stability properties similarly as in the case of systems with interval parameters. On this basis a criterion of stability of linear uncertain systems that is a generalization of the Kharitonov's criterion is provided.

References

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